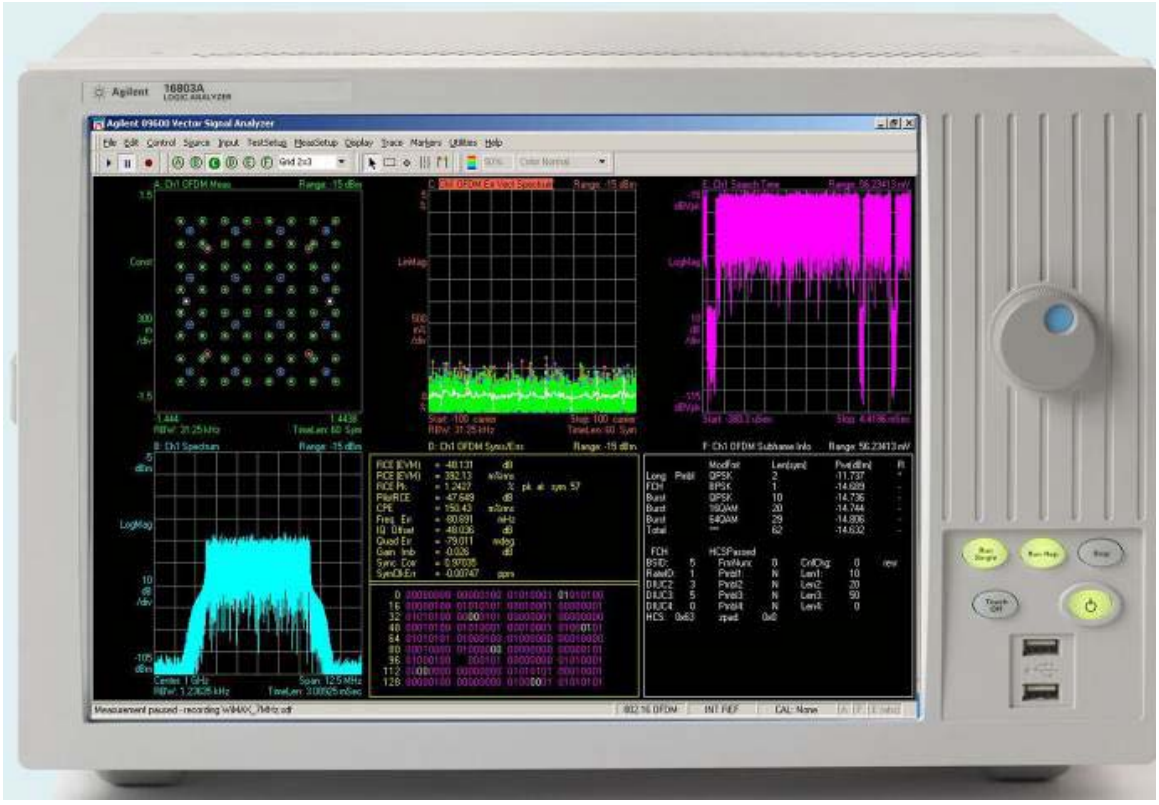
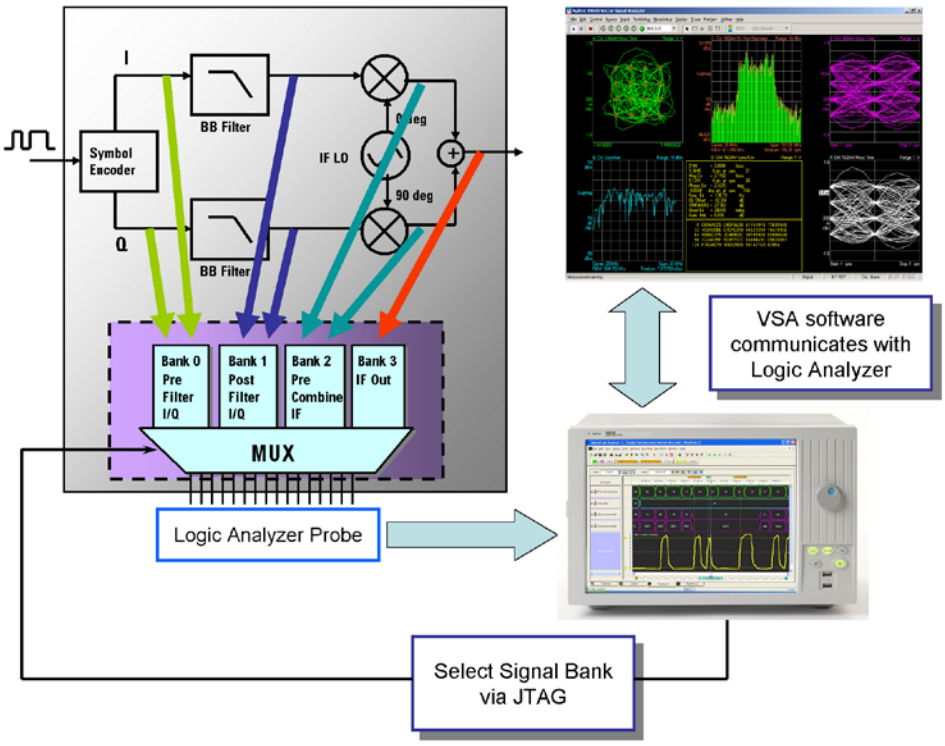
DVSA (Digital Vector Signal Analysis) Demo Guide
(From Signal Studio to VSA)



1 Digital VSA Overview

With the trend in the wireless industry to implement more of the software radio's functionality in the digital domain, the ADC and DAC are moving closer to the antenna. As a result, more of the testing and troubleshooting are performed using a logic analyzer. Bridging the signal formats from analog to digital also requires the ability to correctly interpret the signal value from a digital bus. Some signals use a two's compliment encoding and others use an offset binary encoding, each requiring a different interpretation. Correctly decoding the format of the signal is also important when applying VSA analysis tools directly to logic analyzer measurements. Fortunately, modern VSA tools, such as the Agilent 89600 series, can directly interface with the logic analyzer system software to easily set the encoding format assignments.

How the Digital VSA works?



First, the digital signals (baseband, IF, or RF) are probed with the logic analyzer. In an FPGA, the FPGA dynamic probe is a great way to connect to various parts of the design. In an ASIC or commercial digital RF processing chip, a digital MUX can route baseband and IF signals to chip pads dedicated for debug, which are then connected to the logic analyzer probes. Next, the logic analyzer is configured to capture the signals using synchronous (or "state mode") sampling. Once configured, the VSA software receives digital samples and takes live measurements as a single dedicated instrument.
Refer to the DVSA reference block diagram.

VSA Software Capabilities

You can analyze a wide variety of standard and non-standard signal formats with the VSA software. The VSA software will mostly cover the standard signal presets such as GSM, GSM (EDGE), cdmaOne, cdma2000, W-CDMA, WLAN, WLAN-HT, IEEE-802.16-2004, IEEE-802.16 OFDMA, and many more.
The VSA software will usually provide you the benefits such as:

- Quickly evaluate and troubleshoot digitally modulated signals with the modulation analysis tools.
- Use the constellation and vector diagrams for an overall indication of signal behavior and to obtain clues to the cause of a problem.
- Take advantage of the EVM, EVM spectrum, and EVM time capabilities for a more sensitive examination of signal errors.

2 Related Literature for Digital VSA

Publication Title	Publication Type	Publication No.
Agilent Logic Analyzers and 89601A Vector Signal Analysis Software	Technical Overview	5989-3359EN
How to Measure Digital Baseband and IF Signals Using Agilent Logic Analyzers with 89600 Vector Signal Analysis Softw	Application Note	5989-2384EN
Making RF Measurements on Digital Serial Data with Agilent's Signal Extractor and the 89601A Vector Signal Analyzer	Application Note	5989-5290EN
Software Defined Radio Measurement Solutions	Application Note	5989-6931EN
Agilent 89600 Series Vector Signal Analysis Software 89601A/89601AN/89601N12	Data Sheet	5989-1786EN

3 DVSA Demo Setup Overview

Offline Demo Requirements:

Software

1. Logic Analyzer software version, V3.50 or higher
2. 89601A version, V6.1 or higher
    a. Option 200: Basic vector signal analysis
    b. Option 300: Hardware connectivity
    c. Option AYA: Flexible modulation analysis
3. Look for all the required files in 'Demo Files' folder.

Note: You can do a very simple demo by using the offline data.

a. Open the 'WCDMA IQ16.ala' file. Find the file in 'Demo Files' folder

b. Then, follow Step no.7 to complete the offline demo.

Live Demo Requirements:

Hardware

1. 16800 or 16900 series Logic Analyzer with Pattern Generator
2. Credit Card Demo board x 4
3. Pattern Generator Data Pod x 4
4. Pattern Generator Clock Pod with probe lead set (10498A) x 1

Software

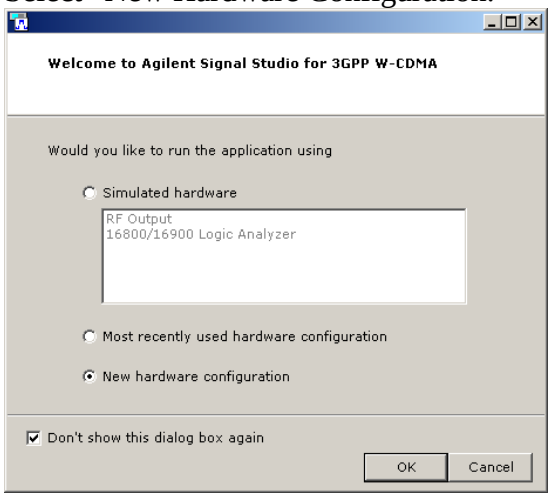
1. Logic Analyzer software version, V3.50 or higher
2. Signal Studio
3. 89601A version, V6.1 or higher
    a. Option 200: Basic vector signal analysis
    b. Option 300: Hardware connectivity
    c. Option AYA: Flexible modulation analysis
4. Signal Inserter

4 Step 1: Generate encrypted waveform files (.wfm) from Signal Studio

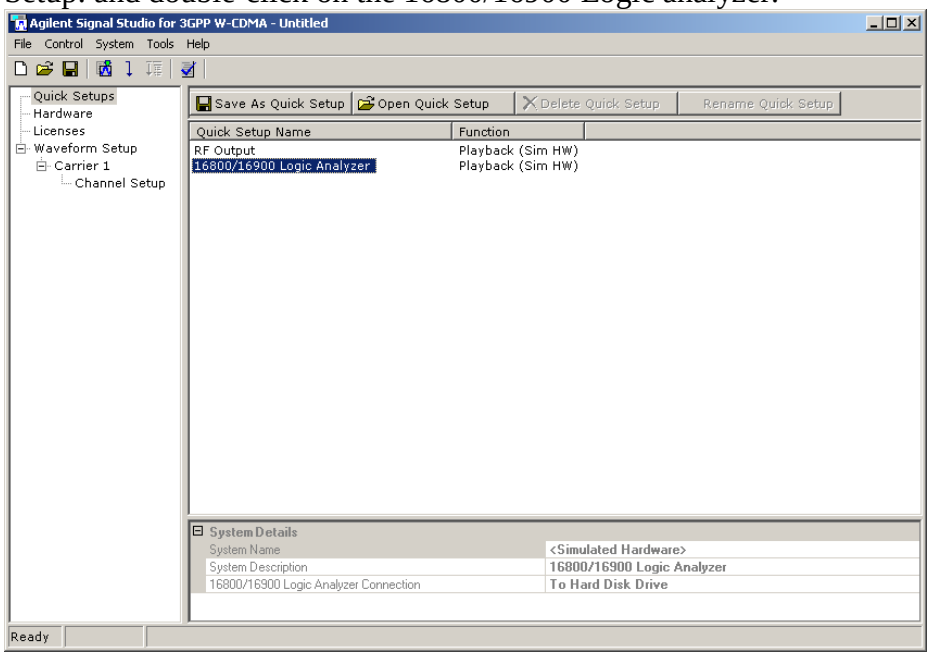
Note: The 'WCDMA TM1 16DPCH.wfm' file is ready in the 'Demo Files' Folder.)

4.1 Double click on the icon.

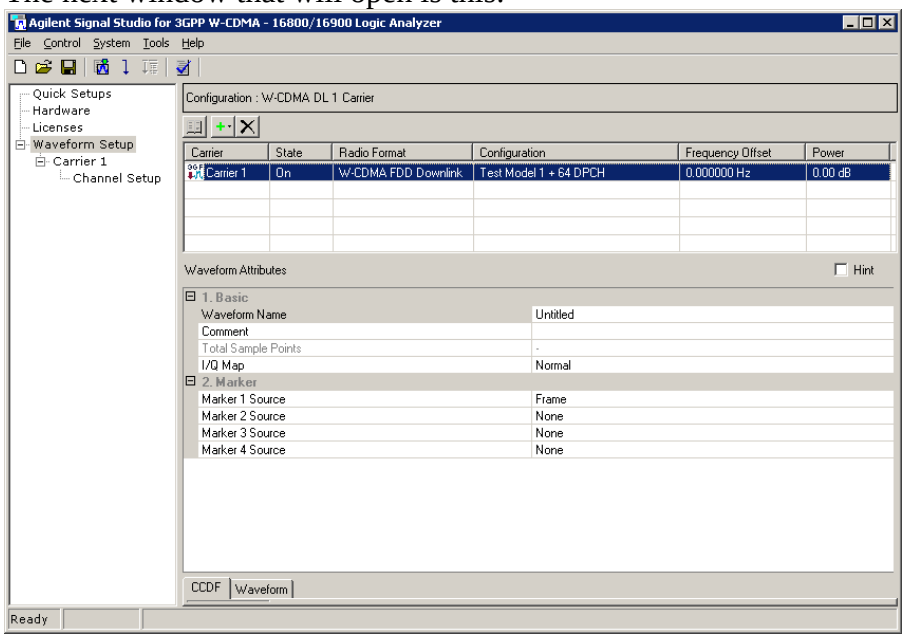
4.1 Select "New Hardware Configuration.



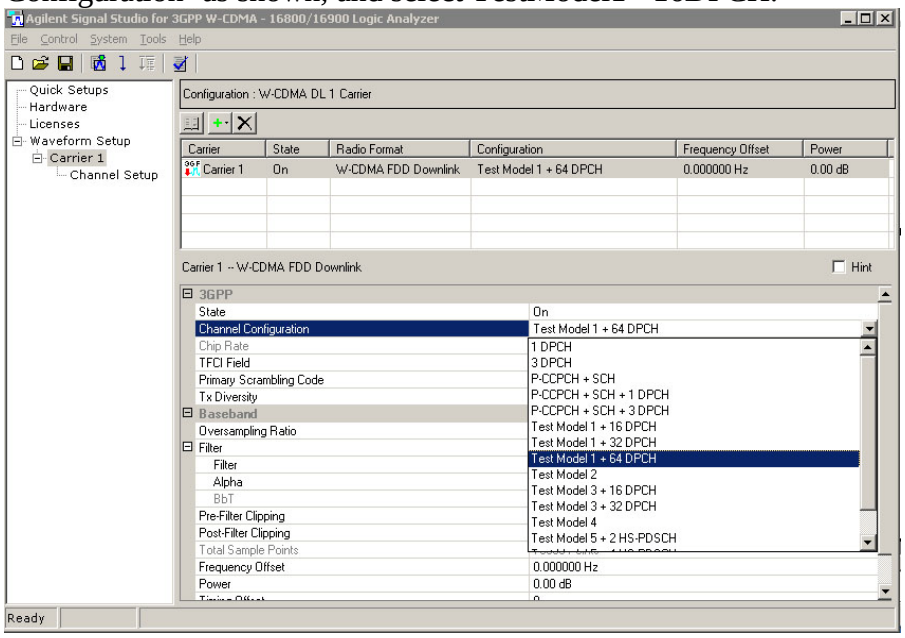
4.2 In some cases the following window will appear. In either case, select "Quick Setup: and double-click on the 16800/16900 Logic analyzer.



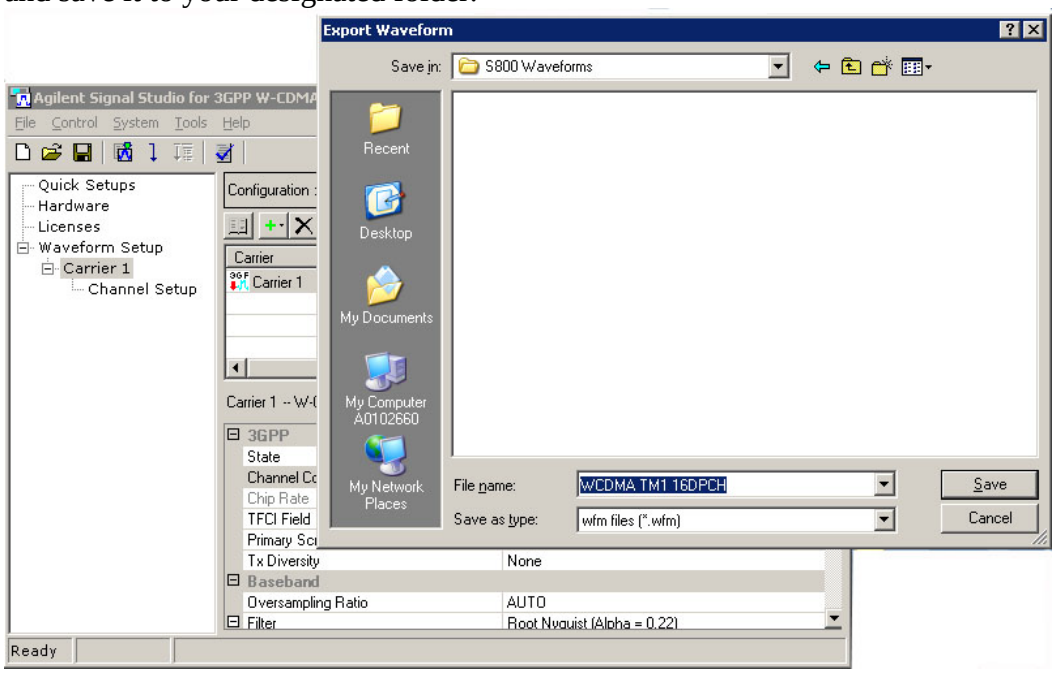
4.3 The next window that will open is this:



4.4 Double-click on 'TestModel1+64DPCH' under the configuration tab to get the window shown in figure below. Pull down the window under 'Channel Configuration' as shown, and select TestModel1 +16DPCH.



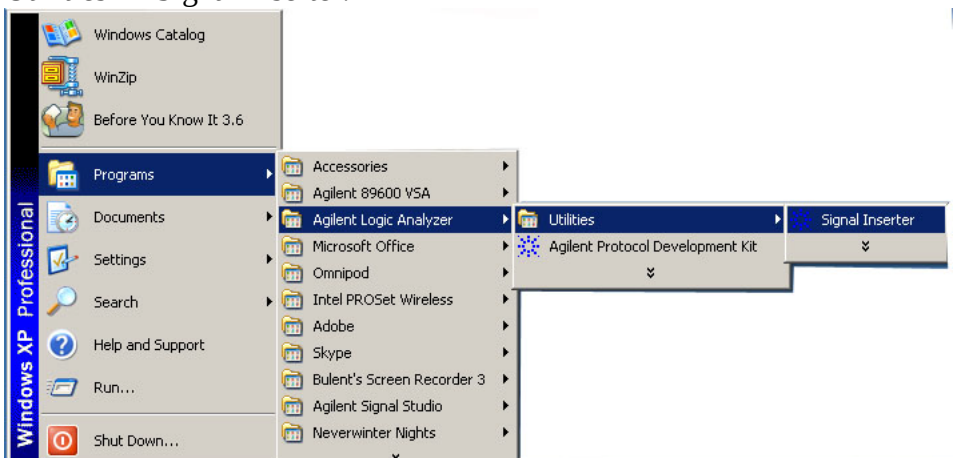
4.5 Select ‘Generate and Download’ and name the file ‘WCDMA TM1 16DPCH’ and save it to your designated folder.



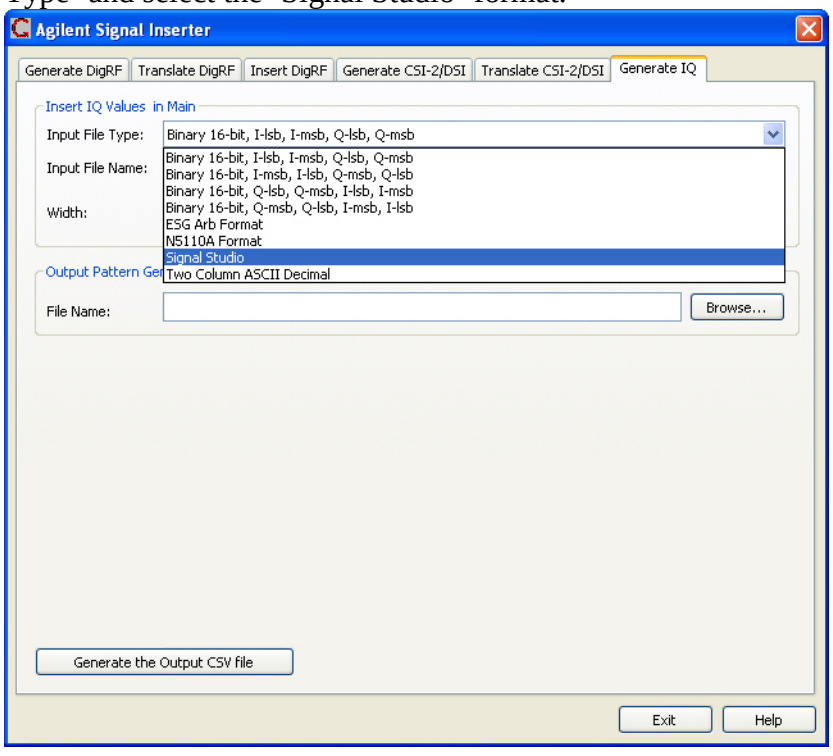
5 Step 2: Generate the Licensed Pattern Generator (.lpg) from Signal Inserter

Note: The 'WCDMA TM1 16DPCH.lpg' file is ready in the 'Demo Files' Folder.

5.1 Open the Signal inserter. Go to Start → All Programs → Logic Analyzer → Utilities → Signal Inserter.

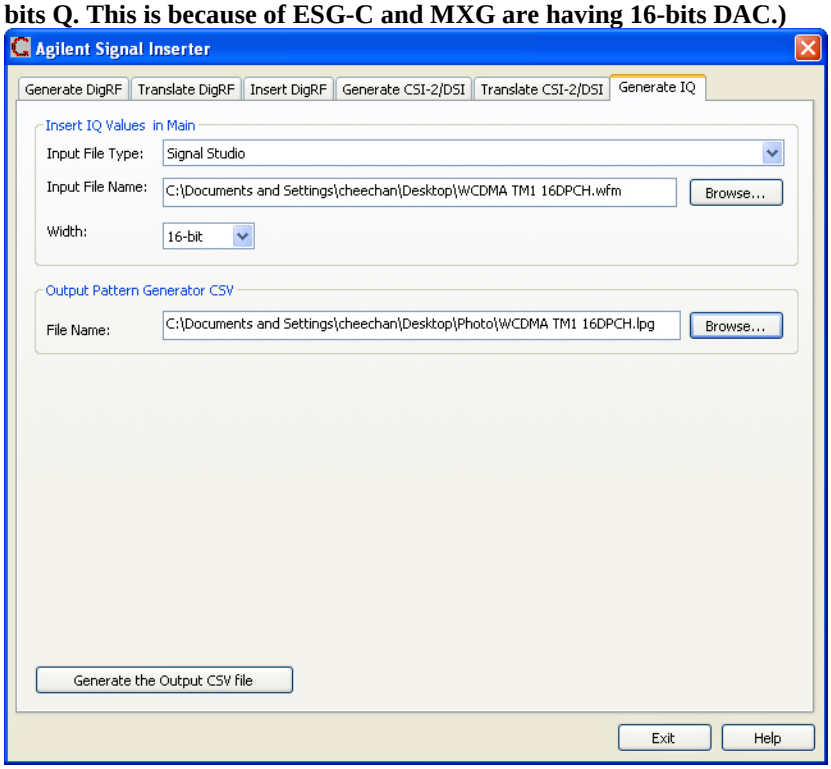


5.2 Select the 'Generate IQ' tab. Using the pull down menu, under the 'Input File Type' and select the 'Signal Studio' format.



5.3 Select the waveform file, WCDMA TM1 16DPCH.wfm by browsing for the file name into the designated folder. Select ’16-bit’ under ‘Width’ to define the IQ bit.

(Note: The waveform which is generated by Signal Studio will consist of 16 bits I and 16 bits Q. This is because of ESG-C and MXG are having 16-bits DAC.)



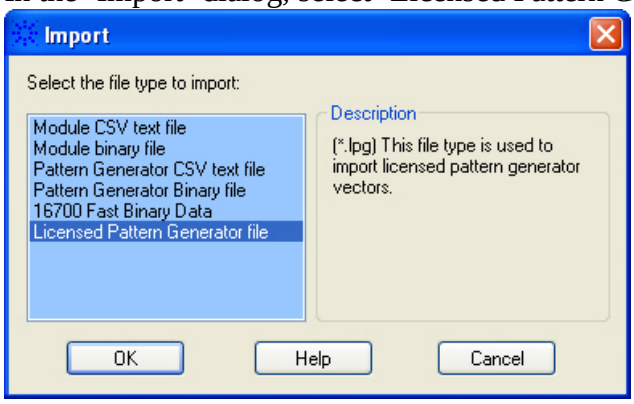
5.4 In the Signal Inserter, under ‘Output Pattern Generator CSV’, select ‘Browse’, browse to the location where you want to save your ‘Licensed Pattern Generator’ (.lpg) file.

5.5 Click on the ‘Generate the Output CSV file’ button to complete the .lpg file generating.

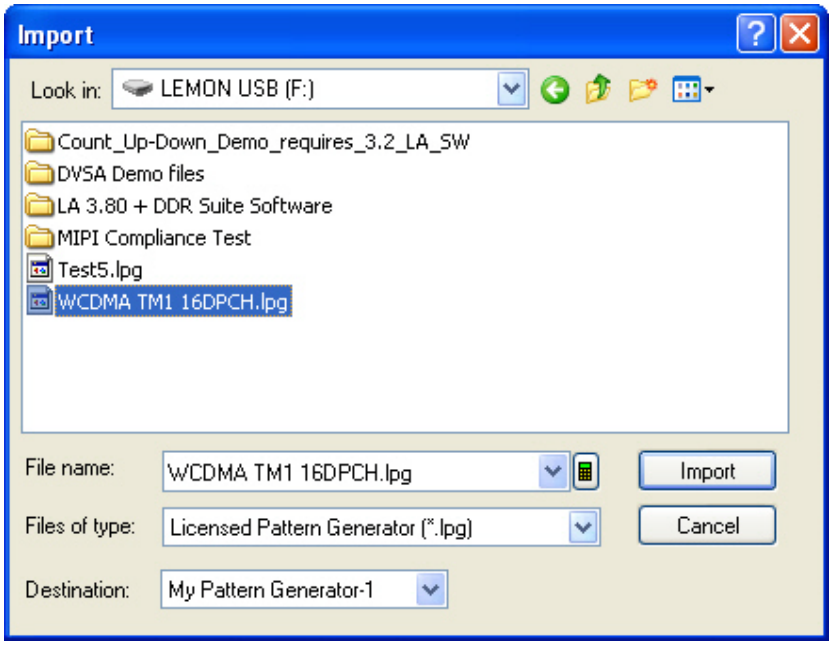
6 Step 3: Import .lpg file to Logic Analyzer Pattern Generator

6.1 From the Agilent Logic Analyzer application's main menu, choose File → Import....

6.2 In the 'Import' dialog, select 'Licensed Pattern Generator file', and click 'OK'.



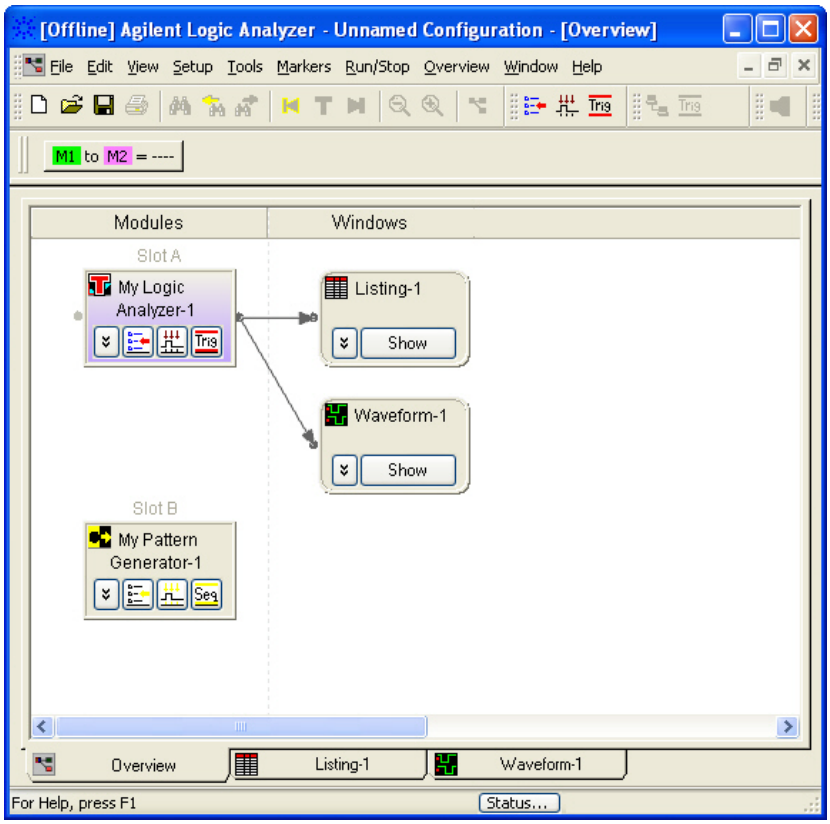
6.3 In the next 'Import' dialog, select the file name of the .lpg file you want to import.



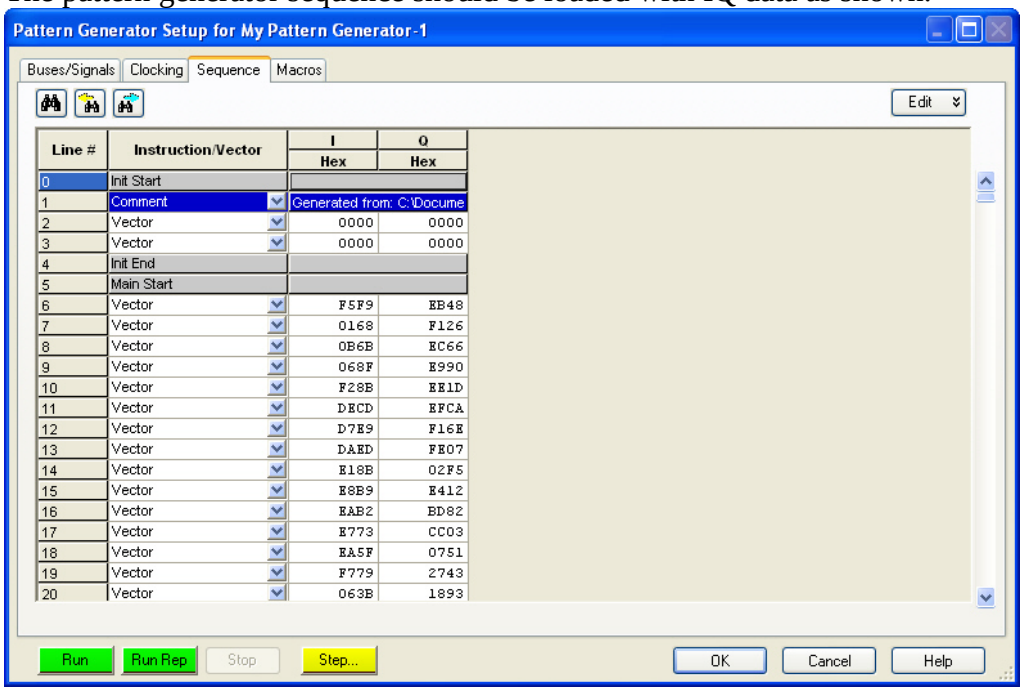
6.4 Select the pattern generator module under 'Destination'.

6.5 Click 'Import' to complete the importing process.

6.6 You may now go to 'Overview' and click on 'Seq' button under Pattern Generator module.

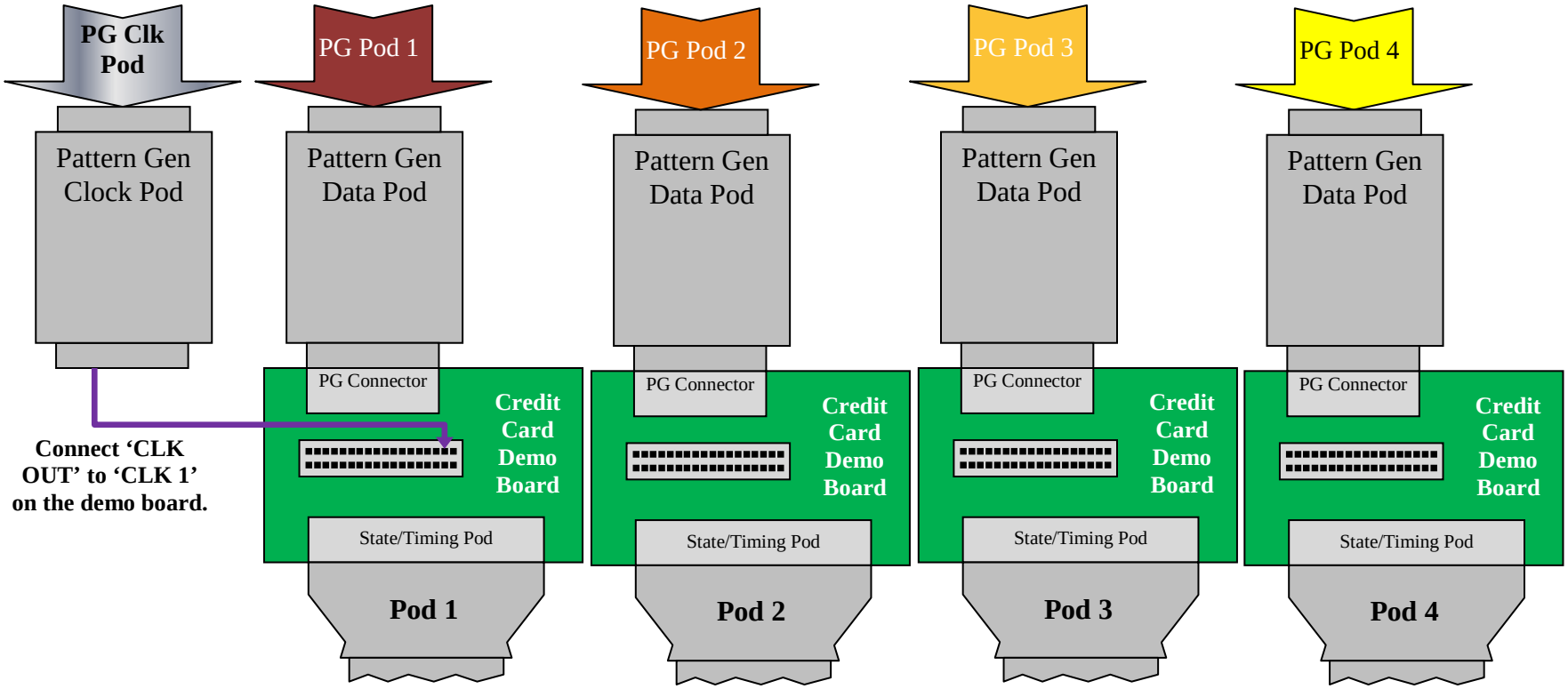


6.7 The pattern generator sequence should be loaded with IQ data as shown.



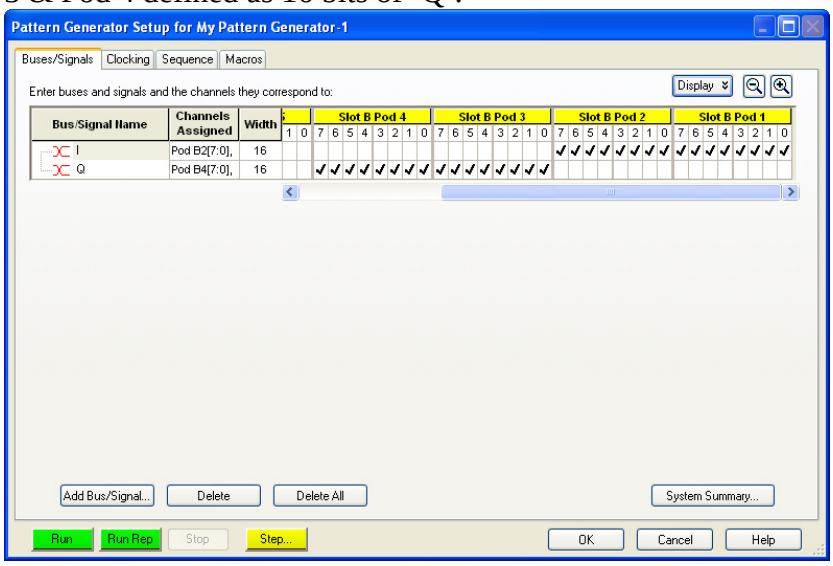
7 Step 4: Hardware Connection

Note: Skip this step if you are not using the same hardware configuration as mentioned in Paragraph no.3 – Live Demo Requirement.

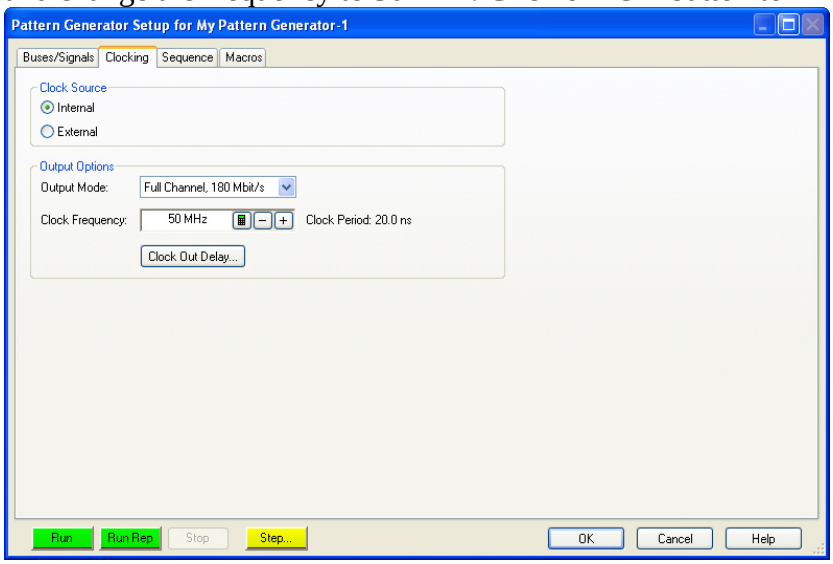


8 Step 5: Setting up pattern generator and sending IQ data

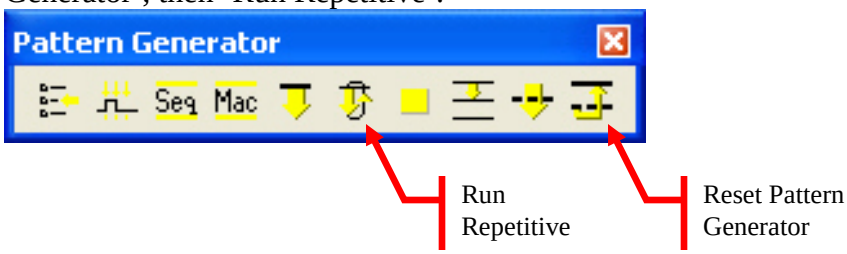
8.1 After loaded .lpg file, pattern generator should be automatically completed the 'Buses/Signal' setup as shown in below and the IQ data should look the same as Step 5.7. Pattern Generator Pod 1 & Pod 2 defined as 16 bits of 'I' and Pod 3 & Pod 4 defined as 16 bits of 'Q'.



8.2 You can now setting up the clocking by selecting the 'Clocking' tab under 'Pattern Generator Setup' window. In this case, we are using 'Internal' clock and change the frequency to 50MHz. Click on 'OK button to finish.



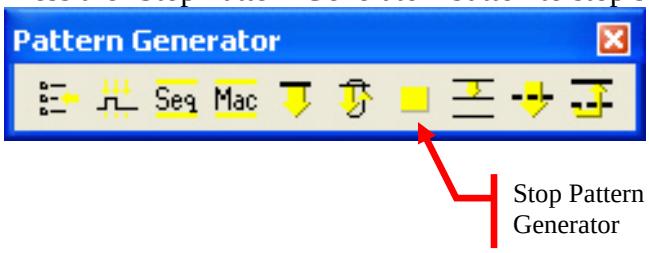
8.3 The pattern generator is ready to send the data. Click on the 'Reset Pattern Generator', then 'Run Repetitive'.



Tips:

a. If you do not see 'Pattern Generator' toolbar on the LA main software then go to main menu and click on View → Toolbars → Pattern Generator.

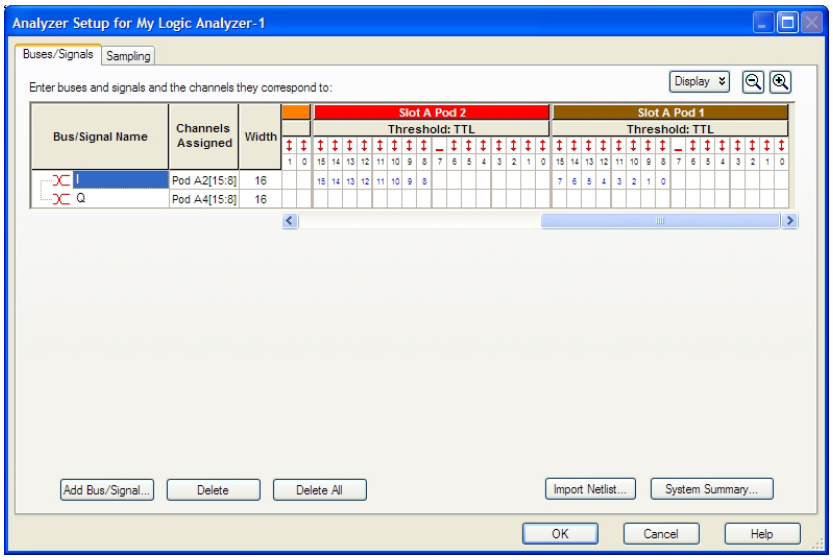
8.4 Press the 'Stop Pattern Generator' button to stop sending data.



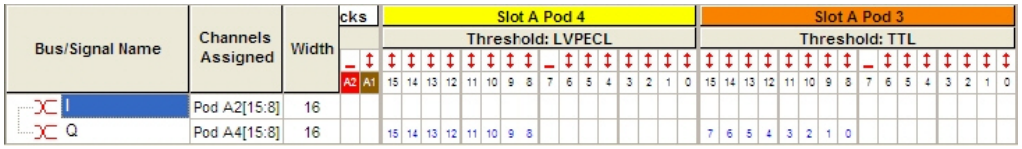
9 Step 6: Setting up logic analyzer to capture IQ data

Note: The settings are only applicable when your hardware connection is followed Step 4.

9.1 The pattern generator should be sending out the IQ output after you completed Step 5. From the Agilent Logic Analyzer application's main menu, choose Setup → Bus/Signal. You will see 8 bits (from bit no.8 till no.15) are activate in each pod (from Pod 1 till Pod 4) you connected to the credit card demo board.



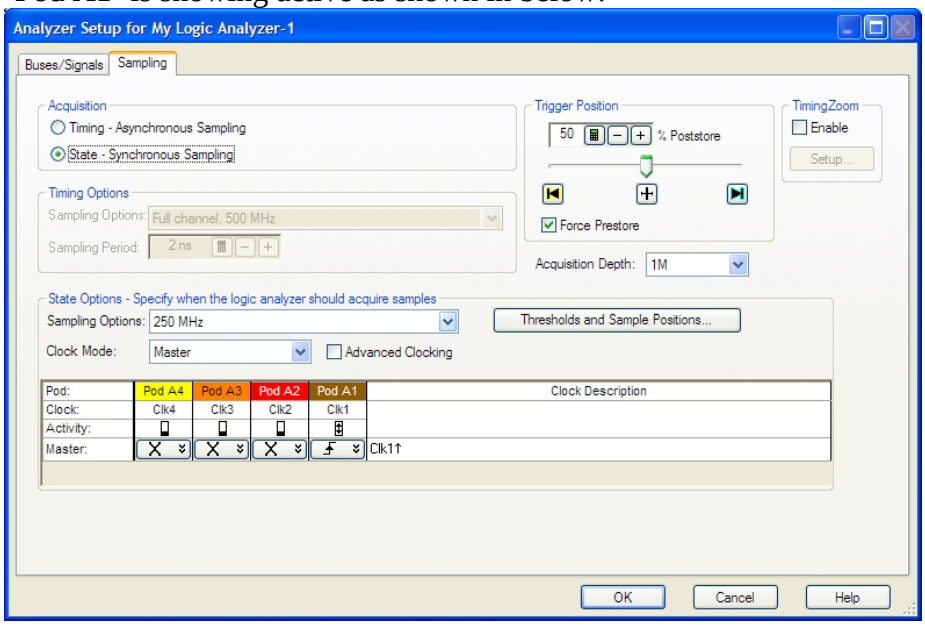
9.2 Define your IQ busses. I = Pod 1, Bit 8~Bit15 and Pod 2, Bit 8~Bit 15 and Q = Pod 3, Bit 8~Bit15 and Pod 4, Bit 8~Bit 15. 'A1' is clock input.



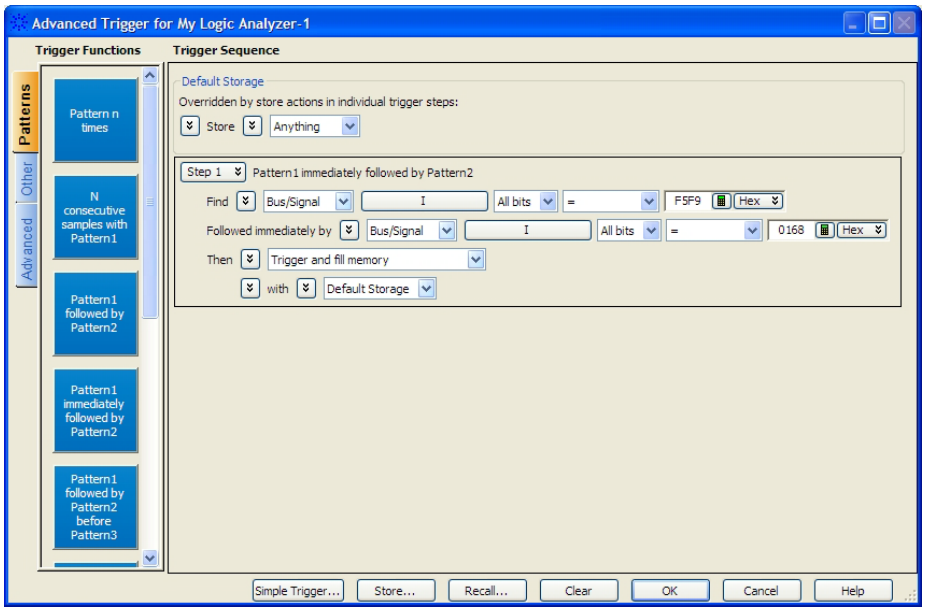
Tips:

a. Right-clicked on the Bus/Signal Name and select 'Enable Channel Order Selection'. This will allow you to define your channel in order.

9.3 From the Agilent Logic Analyzer application's main menu, choose Setup → Timing/State Sampling to define your analysis mode. Select 'State – Synchronous Sampling' under 'Acquisition'. Make sure your 'Clk 1' under 'Pod A1' is showing active as shown in below.



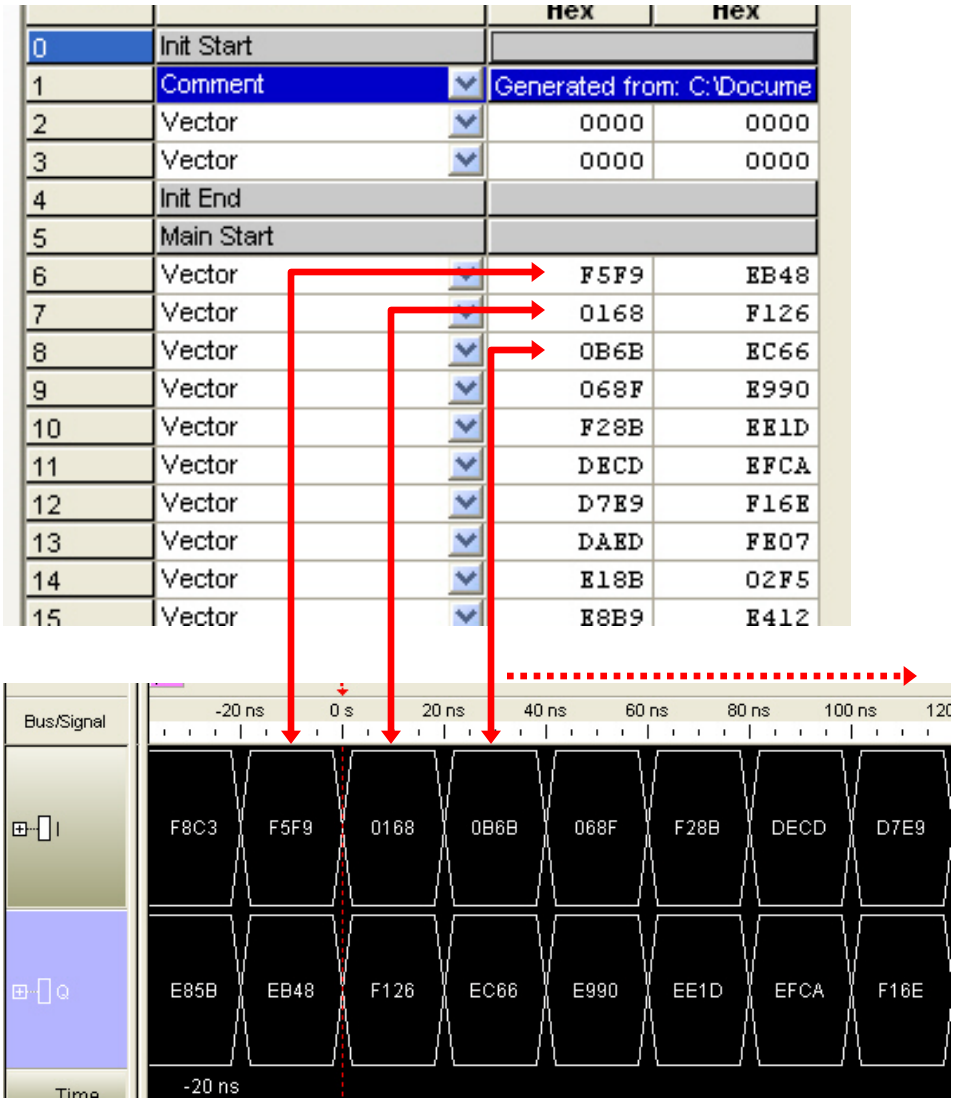
9.4 This step is optional. This is to make sure I trigger on the right location in order for us to confirm on the captured data. In this case, the trigger point will trigger at 'F5F9h' then followed immediately by '0168h' according to the definition in the condition shown below.



Tips:

a. **The LA system will display the result once the memory is filled as default trigger condition.**

b. **The purpose of trigger at 'F5F9h' then followed immediately by '0168h' is because of easy for troubleshooting. The 1st 'I' vector is 'F5F9h' and followed by '0168h', in such a way you can compare the result with your pattern generator vector easily as shown in below.**



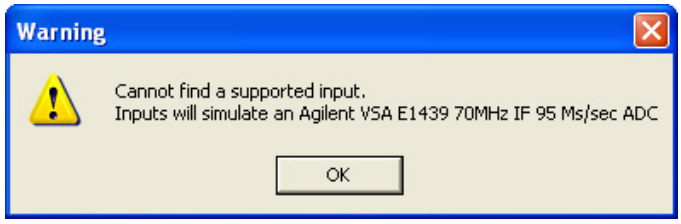
		Hex	Hex
0	Init Start		
1	Comment	Generated from: C:\Docume	
2	Vector	0000	0000
3	Vector	0000	0000
4	Init End		
5	Main Start		
6	Vector	F5F9	EB48
7	Vector	0168	F126
8	Vector	0B6B	EC66
9	Vector	068F	E990
10	Vector	F28B	EE1D
11	Vector	DECD	EFCA
12	Vector	D7E9	F16E
13	Vector	DAED	FE07
14	Vector	E18B	02F5
15	Vector	E8B9	E412

10 Step 7: Glacier Setup and run VSA

10.1 Open the VSA by double-clicking on the ICON.

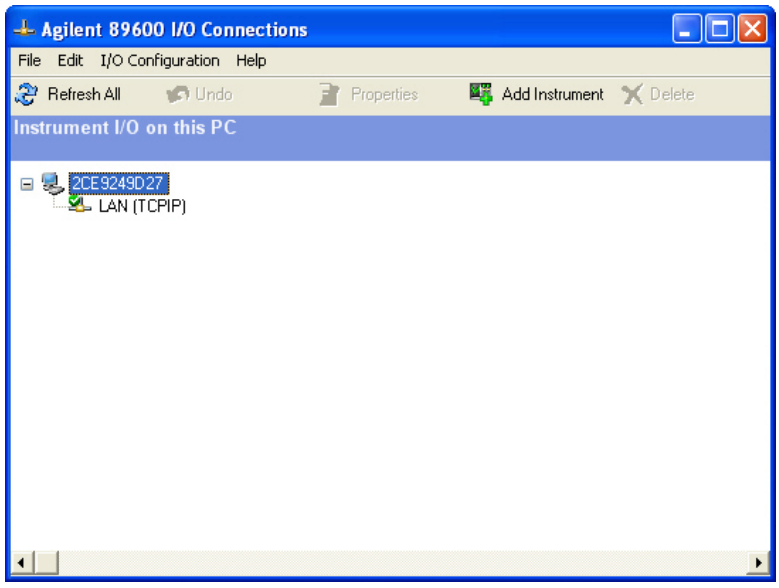
Tips:

a. If you encounter the error shown in below, then follow the following steps to setup the VSA IO Connections.

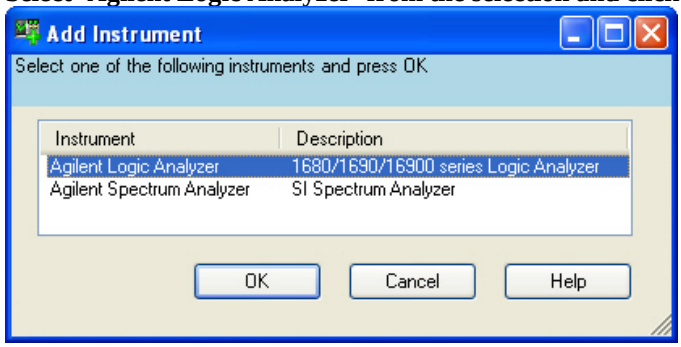


b. Go to Start → All Programs → Agilent 89600 VSA → Logic Analyzer → IO Connections.

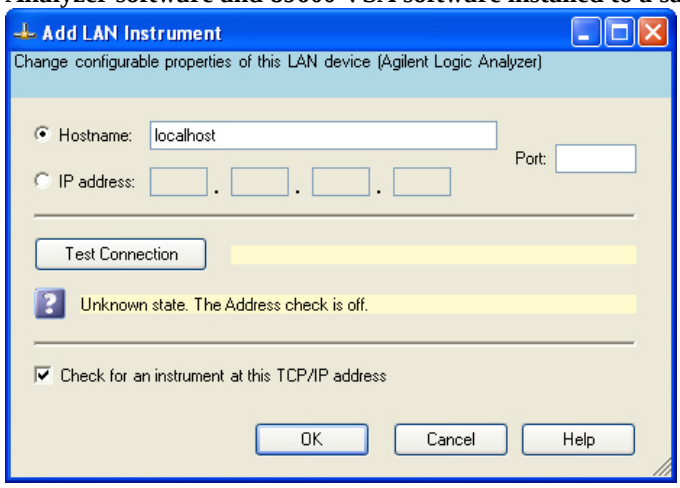
c. Click on the 'Add Instrument'.



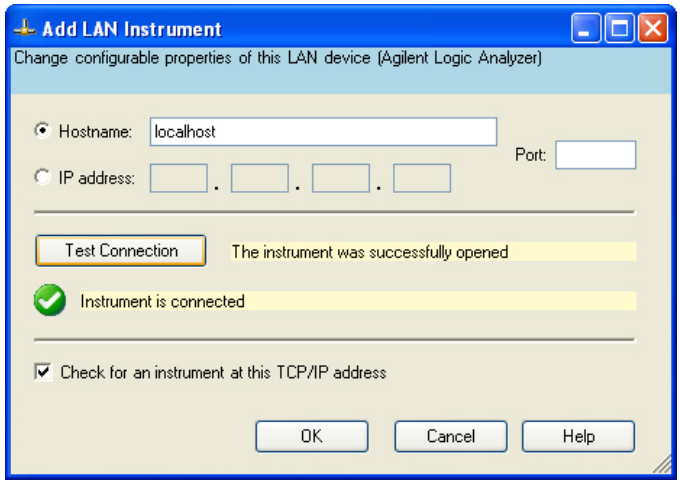
d. Select 'Agilent Logic Analyzer' from the selection and click 'OK' to end the process.



e. Type in 'localhost' under 'Hostname'. 'localhost' is only applicable when the Logic Analyzer software and 89600 VSA software installed to a same controller.

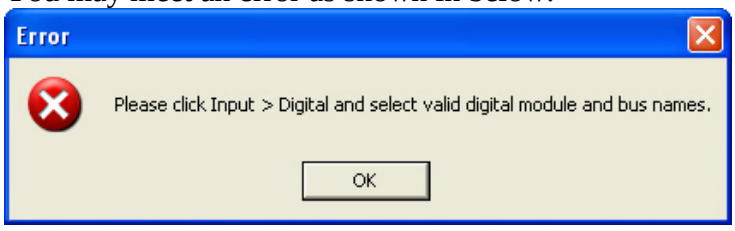


f. Press 'Test Connection' button to check the connectivity. When the status shows 'Instrument is connected' means you are successfully connected Logic Analyzer and VSA software.

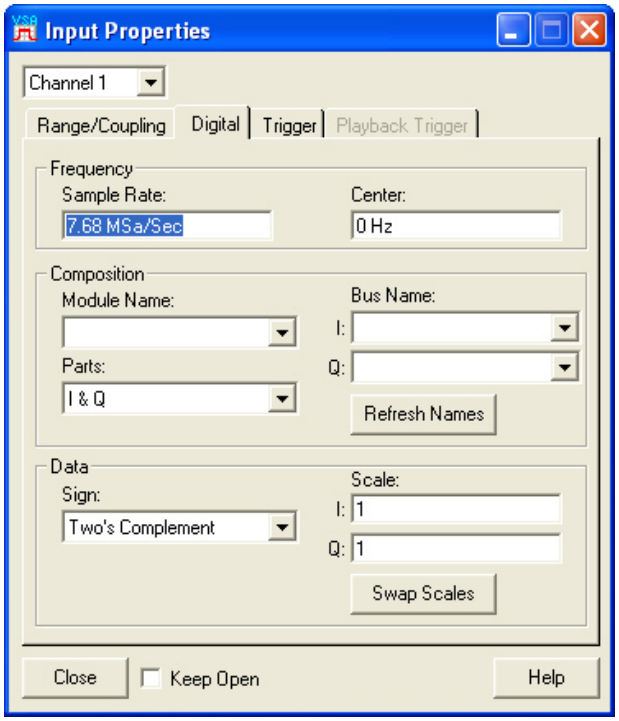


10.2 Go to File → Recall → Recall Setup, and browse to setup file in the 'Demo Files' folder and select the 'wcdma tm1 16 dpch.set' file.

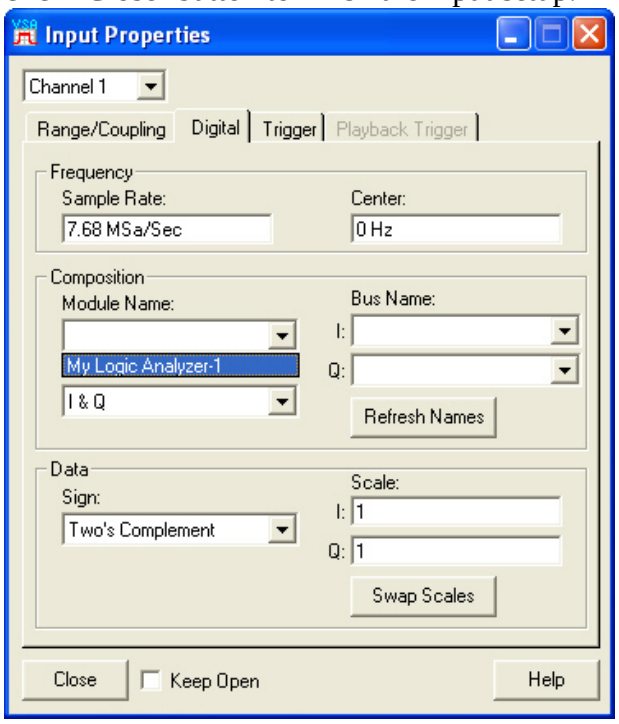
10.3 You may meet an error as shown in below.



10.4 Go to Input → Digital, and check the IQ input. If you unable to see 'My Logic Analyzer-1' in the 'Module Name' column, then click on the 'Refresh Names' button.



10.5 Now, click on the pull down menu and you will see the 'My Logic Analyzer-1' selection appears in the 'Module Name'. Select 'My Logic Analyzer-1' and click 'Close' button to finish the input setup.



10.6 Press  button or go to Control → Restart. Here is what the demodulation looks like.